CLAIMS

What is claimed is:

1. A method of generating a truncated scan test pattern for an integrated circuit design comprising steps of:

(a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

(c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.

2. The method of Claim 1 wherein step (b) comprises generating a set of stuck-at fault test patterns.

3. The method of Claim 2 wherein step (b) comprises ordering the set of stuck-at fault patterns according to fault coverage to generate a set of ordered stuck-at fault patterns.

4. The method of Claim 3 wherein step (b) comprises generating a plot of fault coverage as a function of a number of stuck-at fault patterns from the ordered set of stuck-at fault patterns.

5. The method of Claim 4 wherein step (b) comprises generating a set of transition delay fault patterns for each scan clock domain in the integrated circuit design.

6. The method of Claim 5 wherein step (b) comprises ordering the transition delay fault patterns in the set of transition delay fault patterns for each scan clock domain according to stuck-at fault coverage to generate an ordered set of transition delay fault patterns for each scan clock domain.

7. The method of Claim 6 wherein step (b) comprises ordering each ordered set of transition delay fault patterns according to a number of transition delay fault patterns therein to generate the estimated number of transition delay fault patterns.

8. The method of Claim 7 wherein step (b) comprises generating a plot of transition delay fault coverage as a function of a number of transition delay fault patterns from the total set of transition delay fault patterns.

9. A computer program product for generating a truncated scan test pattern for an integrated circuit design comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

(c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.

10. The computer program product of Claim 9 wherein step (b) comprises generating a set of stuck-at fault test patterns.

11. The computer program product of Claim 10 wherein step (b) comprises ordering the set of stuck-at fault patterns according to fault coverage to generate a set of ordered stuck-at fault patterns.

12. The computer program product of Claim 11 wherein step (b) comprises generating a plot of fault coverage as a function of a number of stuck-at fault patterns from the ordered set of stuck-at fault patterns.

13. The computer program product of Claim 12 wherein step (b) comprises generating a set of transition delay fault patterns for each scan clock domain in the integrated circuit design.

14. The computer program product of Claim 13 wherein step (b) comprises ordering the transition delay fault patterns in the set of transition delay fault patterns for each scan clock domain according to stuck-at fault coverage to generate an ordered set of transition delay fault patterns for each scan clock domain.

15. The computer program product of Claim 14 wherein step (b) comprises ordering each ordered set of transition delay fault patterns according to a number of

transition delay fault patterns therein to generate the estimated number of transition delay fault patterns.

16. The computer program product of Claim 15 wherein step (b) comprises generating a plot of transition delay fault coverage as a function of a number of transition delay fault patterns from the total set of transition delay fault patterns.